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| 09/032,863 | 03/02/1998 | GORDON F. GRIGOR | 0100.01117 | 1397 |

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VEDDER PRICE KAUFMAN & KAMMHOLZ
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| EXAMINER | |
|---|---|
| NGUYEN, KEVIN M | |
| ART UNIT | PAPER NUMBER |
| 2674 | 38 |

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/032,863 | Applicant(s) GRIGOR ET AL. | |
|---|---|---|---|
| | Examiner Kevin M. Nguyen | Art Unit 2674 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *24,29-33,38-53 and 56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24, 29-33, 38-53 and 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Request for Continued Examination*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/28/2004 has been entered. An action on the RCE follows:

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Regarding claims 33 and 38-41, the words "first, second, third, fourth" are preceded by the word "means" in an attempt to use a "means" clause to recite a claim element as a means for performing a specified function. However, since no function is specified by the word(s) preceding "means," it is impossible to determine the equivalents of the element, as required by 35 U.S.C. 112, sixth paragraph. See *Ex parte Klumb*, 159 USPQ 694 (Bd. App. 1967).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24, 29, 31-33, 38, 40-46, 48-52 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zenda (US 4,980,678) hereinafter Zenda '678.

3. *As to claims 24, and 33*, Zenda '678 teaches a video graphics processing circuit associated with a digital storage medium for storing programming instruction, the video graphics processing circuit comprising

a main memory 17 (fig. 1) operably coupled to a processing unit (CPU 1, fig. 1). [recited in claims 24(a)-24(f)]

Zenda '678 teaches recited in col. 5, lines 13-33, for operating in fig. 6A showing the CRT 19 (fig. 1) is chosen to display; recited in col. 5, lines 34-58, for operating in fig. 6B showing that the PDP 21 (fig. 1) to display.

The same reference numerals in Fig 8 denote the same parts as in Fig. 1 (col. 6, lines 18-19).

Thus, Zenda'678 teaches two switches (gates 55, 57) determine whether the memories (main memory 17 and VRAM 15) having a configuration for different resolutions of CRT 19 and PDP 21 to the computing system (computer in fig. 8) can be reconfigured (rewrite memory data from CRT palette data buffer 5 and PDP palette data buffer 7) to maintain effective configuration of the current display of CRT 19 and PDP 21.

Accordingly, Zenda's third embodiment (fig. 8) teaches all of the claimed limitations, except for the display controller simultaneously provides display data to the multiple displays.

However, Zenda's last embodiment (fig. 9) teaches both have CRT 19 and PDP 21 are selectively display-driven (col. 7, lines 65-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Zenda's separate display including simultaneously display for two displays CRT and PDP, in view of the teaching in the last embodiment of Zenda because this would provide an user viewing the both displays CRT and PDP at the same time.

As to claims 29, 38, Zenda '678 teaches CRT 19 and PDP 21 have a separate display controllers (col. 8, lines 55-56).

As to claims 31, 32, 40, 41, Zenda '678 teaches the main memory 17 (fig. 1), screen memories (V-RAM 15, fig. 1) comprise at least a bit maps of V-RAM 15 is screen memory, the V-RAM having a plurality of bit maps, each of bit map storing separate display data (see figure 10, column 7, lines 13-41), and CRT 19 (fig. 1) and PDP 21 (fig. 1) have a separate display controllers (col. 8, lines 55-56).

4. *As to claim 42*, Zenda '678 teaches a video graphics processing circuit comprising:

CRT 19 (fig. 1) and PDP 21 (fig. 1) have a separate display controllers (col. 8, lines 55-56) included on a single video graphics card;

The same reference numerals in Fig. 8 denote the same parts as in Figs 1 and 7 (col. 6, lines 18-19);

two CRT driver 19 and PDP driver 21 (col. 3, lines 46-47);

main memory 17, and screen memories (V-RAM 15, fig. 1) comprise at least a bit maps of V-RAM 15 is screen memory, the V-RAM having a plurality of bit maps, each of bit map storing separate display data (see figure 10, column 7, lines 13-41);

coupling module (gate 55 and gate 57, fig. 8) coupled to two display CRT 19 and PDP 21 and the V-RAM 15;

coupling controller "D-flip flop 59 and decoder 61 (fig. 8) controls switches 55 and 57;"

CRT 19 (fig. 1) and PDP 21 (fig. 1) have a separate display controllers (col. 8, lines 55-56).

Zenda '678 teaches recited in col. 5, lines 13-33, for operating in fig. 6A showing the CRT 19 (fig. 1) is chosen to display; recited in col. 5, lines 34-58, for operating in fig. 6B showing that the PDP 21 (fig. 1) to display.

Accordingly, Zenda's first embodiment (fig. 1) teaches all of the claimed limitations, except for the display controller simultaneously providing display data to the multiple displays.

However, Zenda's last embodiment (fig. 9) teaches both have CRT 19 and PDP 21 are selectively display-driven (col. 7, lines 65-66).

Zenda teaches the operation of last embodiment (fig. 9) will be describes with reference to the flow charts shown in Figs. 11A and 11B (col. 6, lines 57-60);

recited in col. 6, lines 61 through col. 7, line 12, for operating in fig. 11A showing the CRT 19 (fig. 9) is chosen to display;

recited in col. 6, lines 42-64, for operating in fig. 11B showing that the PDP 21 (fig. 9) to display.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Zenda's separate display including simultaneously

display for two displays CRT and PDP, in view of the teaching in the last embodiment of Zenda because this would provide an user viewing the both displays CRT and PDP at the same time.

As to claim 43, Zenda '678 teaches a graphics engine (PD setting control circuit 29 and CRT controller 25) coupling to at least one CRT controller 12 and at least one of the CRT driver 19 (figure 8).

As to claim 44, Zenda '678 teaches a keyboard 16 (user interface, figure 8).

As to claim 45, Zenda '678 teaches BIOS ROM 17, set-up RAM 24 comprising properties memory (CRT pallet data buffer 5 and PDP pallet data buffer 7) that stores configuration properties of two CRT and PDP controllers 12 and 14 and the at least one CRT display 19, wherein the configuration properties include at least one of: limitations of two CRT and PDP controllers 12 and 14 and the at least one CRT display 19 and operational rules of the two CRT and PDP controller 12 and 14 and the at least one CRT display 19 (figure 8, column 6, lines 16-53).

As to claim 46, Zenda '678 teaches a video graphics processing circuit having first display controller 12 coupling to a first display CRT 19, a second display controller 14 coupling to a second display PDP 21 (figure 8, column 6, lines 16-53).

As to claim 48, Zenda '678 teaches a video graphics processing circuit having a first controller 12 and a second controller 14 to one V-RAM 15 (figure 8, column 6, lines 16-53).

5. *As to claim 49*, Zenda '678 teaches a video graphics processing apparatus comprising

screen memories (V-RAM 15, fig. 1) comprise at least a bit maps of V-RAM 15 is screen memory, the V-RAM having a plurality of bit maps, each of bit map storing separate display data (see figure 10, column 7, lines 13-41);

CRT 19 (fig. 1) and PDP 21 (fig. 1) have a separate display controllers (col. 8, lines 55-56);

two CRT driver 19 and PDP driver 21 (col. 3, lines 46-47);

coupling module (gate 55 and gate 57, fig. 8) coupled to two display CRT 19 and PDP 21 and the V-RAM 15;

coupling controller comprises D-flip flop 59 and decoder 61 (fig. 8) controls switches 55 and 57 (fig. 8).

Accordingly, Zenda's first embodiment (fig. 1) teaches all of the claimed limitations, except for the display controller simultaneously providing display data to the multiple displays.

However, Zenda's last embodiment (fig. 9) teaches both have CRT 19 and PDP 21 are selectively display-driven (col. 7, lines 65-66).

Zenda teaches the operation of last embodiment (fig. 9) will be describes with reference to the flow charts shown in Figs. 11A and 11B (col. 6, lines 57-60);

recited in col. 6, lines 61 through col. 7, line 12, for operating in fig. 11A showing the CRT 19 (fig. 9) is chosen to display;

recited in col. 6, lines 42-64, for operating in fig. 11B showing that the PDP 21 (fig. 9) to display.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Zenda's separate display including simultaneously display for two displays CRT and PDP, in view of the teaching in the last embodiment of Zenda because this would provide an user viewing the both displays CRT and PDP at the same time.

As to claim 50, Zenda '678 teaches a graphics engine (PD setting control circuit 29, and CRT controller 25) coupling to plurality of V-RAM 15 (figure 8, column 6, lines 16-53).

As to claim 51, Zenda 678 teaches a user interface 16 (see figure 8).

As to claim 52, Zenda '678 teaches a V-RAM 15 having display refresh rate, display resolution, and type of display (figure 8, column 6, lines 16-53).

As to claim 53, Zenda '678 teaches the coupling controller (59) to couple a first display controller (12) of the plurality of display controllers (12, 14) to a first and a second display of the plurality of displays (19, 21) (see figure 8, column 6, lines 16-53).

As to claim 56, Zenda '678 teaches a controller 25 which couples a V-RAM 15 to more than one of the plurality of display controllers (12, 14) (see figure 8, column 6, lines 16-53).

6. Claims 30, 39 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zenda '678 in view of Zenda (US 5,559,525) hereinafter Zenda '525.

As to claims 30, 39 and 47, Zenda '678 teaches all of the claimed limitations of claims 24, 33, 42, except for "the first display controller couples to a third display."

However, Zenda '525 teaches a related video graphics processing circuit associated with a digital storage medium comprising a display controller (87) coupling a third color CRT (107) (see figure 3A, column 9, lines 8-17).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Zenda '678's display controller providing the display controller (87) coupling the third CRT (107), in view of the teaching in the Zenda '525's reference because this would provide the additional graphics subsystem can be attached and being capable of displaying image data from a built-in graphics subsystem and the optional graphics subsystem on an flat panel display unit as taught by Zenda'525 (col. 2, lines 52-55).

***Response to Arguments***

7. Applicant's arguments filed 01/28/2004 have been fully considered but they are not persuasive.

In response to applicant's argument that claims 24, 33, 42, 49 recite "the display controller simultaneously providing display data to the multiple displays."

This argument is not persuasive because Zenda '678's last embodiment (fig. 9) teaches both have CRT 19 and PDP 21 are selectively display-driven (col. 7, lines 65-66). The operation of last embodiment (fig. 9) will be describes with reference to the flow charts shown in Figs. 11A and 11B (col. 6, lines 57-60); recited in col. 6, lines 61 through col. 7, line 12, for operating in fig. 11A showing the CRT 19 (fig. 9) is chosen to display; recited in col. 6, lines 42-64, for operating in fig. 11B showing that the PDP 21 (fig. 9) to display.

These arguments are not persuasive because the combined teaching of third embodiment (fig. 8) and last embodiment (fig. 9) meet all of the claimed limitations of claims 24, 33, 42 and 49.

In response to applicant's argument that "Examiner has not followed the Supplemental Examination Guidelines for claim under 35 U.S.C. §112, paragraph 6." In response, 35 U.S.C. §112, sixth paragraph has been made in the paragraph 2 above.

For these reasons, the rejections based on Zenda '678 and Zenda '525 have been maintained.

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
March 29, 2004

XIAO WU
PRIMARY EXAMINER